

New Family Displays in Pluspat

New Family Display vs. Individual Family Member Display MMAX

On New Family Display in PlusPat	from Individual Family Member Displays
<p>MMAX</p> <p>1/1 PLUSPAT - (C) QUESTEL-ORBIT Patent Number : EP0613087 A1 19940831 [EP-613087] CA2116314 A1 19940825 [CA2116314] JP6309222 A 19941104 [JP6309222] TW389863 B 20000511 [TW-389863] US5579500 A 19961126 [US5579500]</p> <p>Title of the Invention : (A1) Apparatus and method for achieving high-speed data read access to memory.</p> <p>Patent Assignee : (A1) MATSUSHITA ELECTRIC IND CO LTD (JP)</p> <p>Inventor : (A1) SEKIBE TSUTOMU (JP); KITAMURA TOMOHIRO OCHIAI TOSHIYUKI (JP)</p> <p>Application Data : 1994US-0200217; 1994TW-0101564; 1994CA-2116314; 1994EP-0301250; 1993JP-0353164</p> <p>Priority Details : 1993JP-0035092; 1993JP-0353164</p> <p>IPC (issuing Office) : (A1) G06F-012/02</p> <p>EPO Classification(ECLA) : G06F-012/02C</p> <p>US Class Code : (O) : 711220000; (X) : 711003000</p> <p>Designated States : (EP-613087) DE FR GB</p> <p>Citation : (EP-613087) Cited in the search report EP293720(A)(Cat. X); EP505157(A)(Cat. A) IBM TECHNICAL DISCLOSURE BULLETIN vol. 31, no. 3, August 1988 , NEW YORK US pages 303 - 306 'High performance microprocessor memory system' (Cat. X) Revealed during examination EP604139(A) Citation : (US5579500) US4691277; US4872138; US4914575; US5157776..</p> <p>Abstract of the Invention : (EP-613087) An apparatus and method for controlling data read access to memory, in response to an access request sent through a system bus. The apparatus includes a data storage device for preserving data corresponding to a predetermined address; a judging device for judging whether an access address indicated by the access request matches the predetermined address; and a control device for making the data storage means output data preserved therein to the system bus when the access address has been judged to match the predetermined address, and for making the data storage means hold data corresponding to a next address subsequent to the access address when the access address has been judged not to match the predetermined address.</p>	<p>1/5 PLUSPAT - (C) QUESTEL-ORBIT PN - CA2116314 A1 19940825 [CA2116314] TI - Apparatus and Method for Achieving High-Speed Data Read Access to Memory. PA - (A1) MATSUSHITA ELECTRIC IND CO LTD (JP) AP - CA2116314 19940223 [1994CA-2116314] PR - JP3509293 19930224 [1993JP-0035092]</p> <p>2/5 PLUSPAT - (C) QUESTEL-ORBIT PN - EP0613087 A1 19940831 [EP-613087] TI - (A1) Apparatus and method for achieving high-speed data read access to memory. PA - (A1) MATSUSHITA ELECTRIC IND CO LTD (JP) IN - (A1) SEKIBE TSUTOMU (JP); KITAMURA TOMOHIRO (JP); OCHIAI TOSHIYUKI(JP) AP - EP94301250 19940222 [1994EP-0301250] PR - JP3509293 19930224 [1993JP-0035092] IC - (A1)G06F-012/02 EC - G06F-012/02C DS - DE FR GB CT - Cited in the search report EP293720(A)(Cat. X); EP505157(A)(Cat. A) IBM TECHNICAL DISCLOSURE BULLETIN vol. 31, August 1988 , NEW YORK US pages 303.. AB - An apparatus and method for controlling..</p> <p>3/5 PLUSPAT - (C) QUESTEL-ORBIT PN - JP6309222 A 19941104 [JP6309222] TI - (A) MEMORY CONTROLLER AND METHOD THEREOF PA - (A) MATSUSHITA ELECTRIC IND CO LTD AP - JP35316493 19931228 [1993JP-0353164] PR - JP3509293 19930224 [1993JP-0035092] - JP35316493 19931228 [1993JP-0353164] AB - PURPOSE: To provide the memory controller and memory control method which can read.</p> <p>4/5 PLUSPAT - (C) QUESTEL-ORBIT PN - TW389863 B 20000511 [TW-389863] TI - (B) Memory controller apparatus PA - (B) MATSUSHITA ELECTRIC IND CO LTD (JP) AP - TW83101564 19940223 [1994TW-0101564] PR - JP3509293 19930224 [1993JP-0035092] AB - A memory controller apparatus for controlling data read access...</p> <p>5/5 PLUSPAT - (C) QUESTEL-ORBIT PN - US5579500 A 19961126 [US5579500] TI - (A) Control apparatus for controlling data read accesses to memory.. PA - (A) MATSUSHITA ELECTRIC IND CO LTD (JP) AP - US20021794 19940223 [1994US-0200217] PR - JP3509293 19930224 [1993JP-0035092] EC - G06F-012/02C PCL - (O) : 711220000; (X) : 711003000 CT - US4691277; US4872138; US4914575;.. AB - An apparatus and method for controlling..</p>

New Family Display Formats

MTST	TI OTI IC EC ICO PCL
MSC	TI OTI IC EC ICO PCL
MINI	PN TI PA IN AP PR
MMSS	PN TI OTI PA IN AP PR DS
MSTD	PN TI OTI PA IN AP PR IC EC ICO PCL DS
MASE	PN TI PA IN AP PR AB
MABS	PN TI OTI PA IN AP PR IC EC ICO PCL DS AB
MMAX	PN TI OTI PA IN AP PR IC EC ICO PCL DS CT AB (One Abstract)
MALL	PN TI OTI PA IN AP PR IC EC ICO PCL DS CT AB (All Available Abstracts)
MSTA	PN TI OTI PA IN AP PR IC EC ICO PCL DS AB
MSTE	PN TI PA IN AP PR IC EC ICO PCL DS AB

New Family Display with Other Options

- 1) **Legal Feature:** Display including corresponding Legal Status record(s):
- 2) **Fulltext / Clms Feature:** Display including corresponding Full-text or Claims record(s):
- 3) **Cited Feature:** Display including corresponding Cited record(s):

New Family Display with Legal Status

MFAMSTAT MST A (TI OTI BIB AB) with display of English & non-English **Legal Status** text (**ACT**)
MFAMSTATE MST E (TI BIB AB) with display of English language only **Legal Status** text (**ACTE**)

Examples : New Family Display Formats in PlusPat

MSC / MTST

1/1 PLUSPAT - (C) QUESTEL-ORBIT

Title of the Invention:

- (A) Control apparatus for controlling data read accesses to memory and subsequent address generation scheme based on data/memory width determination and address validation

Other Title:

- (A1) Dispositif et proc'ed'e d'acc'es rapide de lecture `a m'emoire.
- (A1) Vorrichtung und Verfahren zum Speicherleszugriff mit hoher Geschwindigkeit.

IPC (issuing Office):

- (A) G06F-012/02

EPO Classification(ECLA):

- G06F-012/02C

US Class Code:

- ORIGINAL (O) : 711220000; CROSS-REFERENCE (X) : 711003000

MSTD

1/1 PLUSPAT - (C) QUESTEL-ORBIT

Patent Number:

- US5579500 A 19961126 [US5579500]
- CA2116314 A1 19940825 [CA2116314]
- EP0613087 A1 19940831 [EP-613087]
- JP6309222 A 19941104 [JP06309222]
- TW389863 B 20000511 [TW-389863]

Title of the Invention:

- (A) Control apparatus for controlling data read accesses to memory and subsequent address generation scheme based on data/memory width determination and address validation

Other Title:

- (A1) Dispositif et proc'ed'e d'acc'es rapide de lecture `a m'emoire.
- (A1) Vorrichtung und Verfahren zum Speicherleszugriff mit hoher Geschwindigkeit.

Patent Assignee:

- (A) MATSUSHITA ELECTRIC IND CO LTD (JP)

Inventor:

- (A) SEKIBE TSUTOMU (JP); KITAMURA TOMOHIKO (JP); OCHIAI TOSHIYUKI (JP)

Application Data:

1994US-0200217; 1994TW-0101564; 1994CA-2116314;
1994EP-0301250; 1993JP-0353164

Priority Details:

1993JP-0035092; 1993JP-0353164

IPC (issuing Office):

- (A) G06F-012/02

EPO Classification(ECLA):

- G06F-012/02C

US Class Code:

- ORIGINAL (O) : 711220000; CROSS-REFERENCE (X) : 711003000

Designated States:

(EP-613087)
DE FR GB

Examples : New Family Display Formats in PlusPat

MINI LEGAL

1/1 PLUSPAT - (C) QUESTEL-ORBIT

Patent Number:

- US5579500 A 19961126 [US5579500]
- CA2116314 A1 19940825 [CA2116314]
- EP0613087 A1 19940831 [EP-613087]
- JP6309222 A 19941104 [JP06309222]
- TW389863 B 20000511 [TW-389863]

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- (A) Control apparatus for controlling data read accesses to memory and subsequent address generation scheme based on data/memory width determination and address validation

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Inventor:

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Application Data:

1994US-0200217; 1994TW-0101564; 1994CA-2116314;
1994EP-0301250; 1993JP-0353164

Priority Details:

1993JP-0035092; 1993JP-0353164

1/2 LGST - (C) LEGSTAT

Patent Number:

- US 5579500 [US5579500]

Application Number:

- US 200217/94 19940223 [1994US-0200217]

Document Type:

- US-P

Action Taken:

- 19940223 US/AE-A
APPLICATION DATA (PATENT)
{US 200217/94 19940223 [1994US-0200217]}
- 19940407 US/AS02
ASSIGNMENT OF ASSIGNOR'S INTEREST
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. 1006, OAZA
- 19961126 US/A PATENT

2/2 LGST - (C) LEGSTAT

Patent Number:

- EP 613087 [EP-613087]

Application Number:

- EP 94301250/94 19940222 [1994EP-0301250]

Document Type:

- EP-P

Action Taken:

- 19940222 EP/AE-A
EP-APPLICATION
EUROPAEISCHE ANMELDUNG
{EP 94301250/94 19940222 [1994EP-0301250]}
- 19940831 EP/AK-A1 [+]
DESIGNATED CONTRACTING STATES IN AN APPLICATION WITH SEARCH REPORT:
IN EINER ANMELDUNG BENANNTE VERTRAGSSTAATEN
DE FR GB
:
- 19950426 EP/17P [+]
REQUEST FOR EXAMINATION FILED
PRUEFUNGSANTRAG GESTELLT
950224
- 20000322 EP/17Q [+]
FIRST EXAMINATION REPORT
ERSTER PRUEFUNGSBESCHEID
20000204

Examples : New Family Display Formats in PlusPat

MASE FULLEPO CLM

1/1 PLUSPAT - (C) QUESTEL-ORBIT

Patent Number:

- US5579500 A 19961126 [US5579500]
- CA2116314 A1 19940825 [CA2116314]
- EP0613087 A1 19940831 [EP-613087]
- JP6309222 A 19941104 [JP06309222]
- TW389863 B 20000511 [TW-389863]

Title of the Invention:

- (A) Control apparatus for controlling data read accesses to memory and subsequent address generation scheme based on data/memory width determination and address validation

Patent Assignee:

- (A) MATSUSHITA ELECTRIC IND CO LTD (JP)

Inventor:

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Application Data:

1994US-0200217; 1994TW-0101564; 1994CA-2116314;
1994EP-0301250; 1993JP-0353164

Priority Details:

1993JP-0035092; 1993JP-0353164

Abstract of the Invention:

- (US5579500)

An apparatus and method for controlling data read access to memory, in response to an access request sent through a system bus. The apparatus includes an data storage device for preserving data corresponding to a predetermined address; a judging device for judging whether an access address indicated by the access request matches the predetermined address; and a control device for making the data storage device output data preserved therein to the system bus when the access address has been judged to match the predetermined address, and for making the data storage device hold data corresponding to a next address subsequent to the access address when the access address has been judged not to match the predetermined address.

Claims: - (EP0613087) EPAPAT - (C) INPI/OEB

1. An apparatus for controlling data read access to memory, in response to an access request sent through a system bus, comprising:

a data storage means for preserving data corresponding to a predetermined address;

a judging means for judging whether an access address indicated by said access request matches the predetermined address; and

a control means for making said data storage means output data preserved therein to the system bus when said access address has been judged to match the predetermined address, and for making said data storage means hold data corresponding to a next address subsequent to said access address when said access address has been judged not to match the predetermined address.

:

:

22. The method of claim 21, wherein said next address indicates data subsequent to data corresponding to said access address, said data indicated by said next address having a same data width as said memory.

Examples : New Family Display Formats in PlusPat

MSTE CITALL

1/1 PLUSPAT - (C) QUESTEL-ORBIT

Patent Number:

US5579500 A 19961126 [US5579500]
CA2116314 A1 19940825 [CA2116314]
EP0613087 A1 19940831 [EP-613087]
JP6309222 A 19941104 [JP06309222]
TW389863 B 20000511 [TW-389863]

Title of the Invention:

(A) Control apparatus for controlling data read accesses to memory and subsequent address generation scheme based on data/memory width determination and address validation

Patent Assignee:

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Inventor:

- (A) SEKIBE TSUTOMU (JP); KITAMURA TOMOHIKO (JP); OCHIAI TOSHIYUKI (JP)

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1993JP-0035092; 1993JP-0353164

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- (A) G06F-012/02

EPO Classification(ECLA):

- G06F-012/02C

US Class Code:

- ORIGINAL (O) : 711220000; CROSS-REFERENCE (X) : 711003000

Designated States:

(EP-613087)

DE FR GB

Abstract of the Invention:

- (US5579500)

An apparatus and method for controlling data read access to memory, in response to an access request sent

:

subsequent to the access address when the access address has been judged not to match the predetermined address.

1/1 EPAT - (C) INPI/OEB- image

Public. Number:

- EP613087 A1 19940831 [EP-613087]

Search Report:

- Cited in the search report
- EP293720(A)(Cat. X) EP505157(A)(Cat. A)
- IBM TECHNICAL DISCLOSURE BULLETIN vol. 31, no. 3 , August 1988 , NEW YORK US pages 303 - 306 'High performance microprocessor memory system'(Cat. X)
- Revealed during examination
- EP604139(A)

RR Bulletin:

- 1994-35

Date R. Report:

- 1994-08-31 Search report

1/1 USPAT - (C) USPTO

Patent Number:

- ***US5579500*** A 19961126

Cited Patents:

- US4691277 19870900 [US4691277] 395421030 Kronstadt et al.
US4872138 19891000 [US4872138] 365049000 Ciacci
US4914575 19900400 [US4914575] 395484000 Kihara et al.
US5157776 19921000 [US5157776] 395458000 Foster
EP0293720 19880500 [EP-293720]
EP0505157 19920300 [EP-505157]
JP60-24663 19850200 [JP60024663]
JP60-221857 19851100 [JP60221857]
JP63-89954 19880400 [JP63089954]
JP63-271647 19881100 [JP63271647]

Other Patent References:

- IBM Technical Disclosure Bulletin, vol. 31, No. 3,.....

Examples : New Family Display Formats in PlusPat

MFAMSTATE

1/1 PLUSPAT - (C) QUESTEL-ORBIT

Patent Number:

US5579500 A 19961126 [US5579500]
CA2116314 A1 19940825 [CA2116314]
EP0613087 A1 19940831 [EP-613087]
JP6309222 A 19941104 [JP06309222]
TW389863 B 20000511 [TW-389863]

Title of the Invention:

(A) Control apparatus for controlling data read accesses to memory and subsequent address generation scheme based on data/memory width determination and address validation

Patent Assignee:

- (A) MATSUSHITA ELECTRIC IND CO LTD (JP)

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- (A) SEKIBE TSUTOMU (JP); KITAMURA TOMOHIKO (JP); OCHIAI TOSHIYUKI (JP)

Application Data:

1994US-0200217; 1994TW-0101564; 1994CA-2116314; 1994EP-0301250; 1993JP-0353164

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1993JP-0035092; 1993JP-0353164

IPC (issuing Office):

- (A) G06F-012/02

EPO Classification(ECLA):

- G06F-012/02C

US Class Code:

- ORIGINAL (O) : 711220000; CROSS-REFERENCE (X) : 711003000

Designated States:

(EP-613087)

DE FR GB

Abstract of the Invention:

- (US5579500)

An apparatus and method for controlling data read access to memory, in response to an access request sent

:
:

subsequent to the access address when the access address has been judged not to match the predetermined address.

(US5579500) LEGALI (C) LEGSTAT

19940223 US/AE-A

APPLICATION DATA (PATENT)

{US 200217/94 19940223 [1994US-0200217]}

- 19940407 US/AS02

ASSIGNMENT OF ASSIGNOR'S INTEREST

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. 1006, OAZA

KADOMA KADOMA-SHI, OSAKA-FU, * SEKIBE, TSUTOMU :

19940218; KITAMURA, TOMOHIKO : 19940218; OCHIAI,

TOSHIYUKI : 19940218

- 19961126 US/A

PATENT

(EP-613087) LEGALI (C) LEGSTAT

19940222 EP/AE-A

EP-APPLICATION

{EP 94301250/94 19940222 [1994EP-0301250]}

- 19940831 EP/AK-A1 [+]

DESIGNATED CONTRACTING STATES IN AN APPLICATION WITH

SEARCH REPORT:

DE FR GB

- 19940831 EP/A1 [+]

PUBLICATION OF APPLICATION WITH SEARCH REPORT

- 19950426 EP/17P [+]

REQUEST FOR EXAMINATION FILED

950224

- 20000322 EP/17Q [+]

FIRST EXAMINATION REPORT

20000204

STATISTICAL ANALYSIS : GET / MEMS on Family Results set

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1/1 ECLATX - (C) INPI/OEB
GR G06F-009/00 Arrangements for programme control, e.g. control unit
SD05 .. G06F-009/46 Multiprogramming arrangements, e.g. using interrupt;..
... G06F-009/46A [N: Allocation of resources, e.g. of CPU] [N9704]
.... G06F-009/46A4 [N: Software resources, e.g. task allocation
..... G06F-009/46A4L [N: Load balancing] [N9704]
```

File : PLUSPAT

SS Results

1 352 /EC G06F-009/46A4L

Search statement 2

?get pa top 10

Total number of terms extracted: 139

Number of terms now in MEM2 : 10

Memory is of type MEMSORT (statistical analysis)

#	FREQ		TERM
1	22	6.25%	IBM
2	13	3.69%	HITACHI LTD
3	9	2.55%	MITSUBISHI ELECTRIC CORP
4	8	2.27%	BULL SA
5	6	1.70%	FUJITSU LTD
6	6	1.70%	LUCENT TECHNOLOGIES INC
7	6	1.70%	NIPPON TELEGRAPH & TELEPHONE
8	4	1.13%	EMC CORP
9	4	1.13%	SIEMENS AG
10	4	1.13%	TOKYO SHIBAURA ELECTRIC CO

?fam ss 1

306 Patent Groups

** SS 2: Results 494

get pa top 10

Total number of terms extracted: 286

Number of terms now in MEM2 : 10

Memory is of type MEMSORT (statistical analysis)

#	FREQ		TERM
1	15	4.90%	IBM
2	11	3.59%	HITACHI LTD
3	5	1.63%	FUJITSU LTD
4	4	1.30%	LUCENT TECHNOLOGIES INC
5	3	0.98%	AT & T BELL LAB
6	3	0.98%	AT & T CORP
7	3	0.98%	BULL SA
8	3	0.98%	MITSUBISHI ELECTRIC CORP
9	3	0.98%	NIPPON ELECTRIC CO
10	2	0.65%	AMERICAN TELEPHONE & TELEGRAPH